OWNER'S MANUAL

Model 2718

Serial / Parallel I / O Interface

California Computer Systems

CCS MODEL 2718

PARALLEL/SERIAL INTERFACE

OWNER'S MANUAL

Rev. A
Manual #89000-02718

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CHAPTER 1

THEORY OF OPERATION

The CCS Model 2718 is a highly flexible I/O interface board featuring two serial ports and two parallel ports, with full handshaking for each port. Of the serial ports, one is asynchronous (a UART), while the other can be programmed to be synchronous or asynchronous (a USART). Both provide considerable format selectability, the UART through hardware, the USART through software. The interface for each serial port conforms to the EIA RS-232-C specifications, while each parallel port includes a full four-line handshaking scheme, with jumpers allowing selection of the sense polarity of the individual lines. The base addresses of the serial ports, the parallel ports, and an optional (user-supplied) 2K ROM are also jumper-selectable.

This chapter describes in general the circuitry of the 2718. For clarification and greater detail, see the schematic/logic diagram, Section A.9, and the block diagram on page 1-3. Throughout the manual, a low-active signal is indicated by an asterisk after the signal name/mnemonic (e.g., pWR*), or by a bar over the name/mnemonic.

1.1 PORT ADDRESSING

The PAR ADDR and SER ADDR jumpers allow selection of the base addresses of the 2718's parallel and serial ports. The serial ports occupy four sequential addresses, the base address being set on SER ADDR jumpers 2-7 to any multiple of 4 within the S-100's block of 256 I/O ports. The parallel ports occupy two sequential addresses, PAR ADDR jumpers 1-7 determining the base address at any multiple of 2 between 0 and 255.

The internal signal PUP (Parallel Up) is active when address bits A1-A7 match the PAR ADDR jumper settings and the I/O signal (sINP ORed with sOUT) is high. If, when PUP is high, either pWR* or sINP is high (indicating a data transfer operation), the Parallel Port Decoder (U8B) is enabled. A0 then determines whether port A or port B is addressed, while sOUT determines whether an input or output latch is enabled (see Table 1.1.)

If address bits A2-A7 match the SER ADDR jumper settings while I/O is active and PUP is low, SUP (Serial Up) will be high. When SUP is high, the condition of A1 determines whether the UART or the USART is selected. Separate A0 and pWR/sOUT inputs control register addressing for each port (see Tables 1.2 and 1.3). Jumpers SPR, SAI, and SBI allow the sense polarity of A1 and the separate A0 inputs to each serial port to be inverted (see Sections 2.1.2 and 2.1.3). In the tables below and throughout this chapter it is assumed that A1 and A0 are not inverted.

A0	sOUT	REGISTER
0	0	Par A Output
0	1	Par A Input
1	0	Par B Output
1	1	Par B Input

PARALLEL PORTS

TABLE 1.1

A0	$\overline{pWR}$	REGISTER
0	0	Baud Rate
0	1	Ser A/Par Status
1	0	UART Transmitter
1	1	UART Receiver

SERIAL PORT A

TABLE 1.2

A0	$\overline{pWR}$	REGISTER
0	0	USART Transmitter
0	1	USART Receiver
1	0	USART Command
1	1	USART Status

SERIAL PORT B

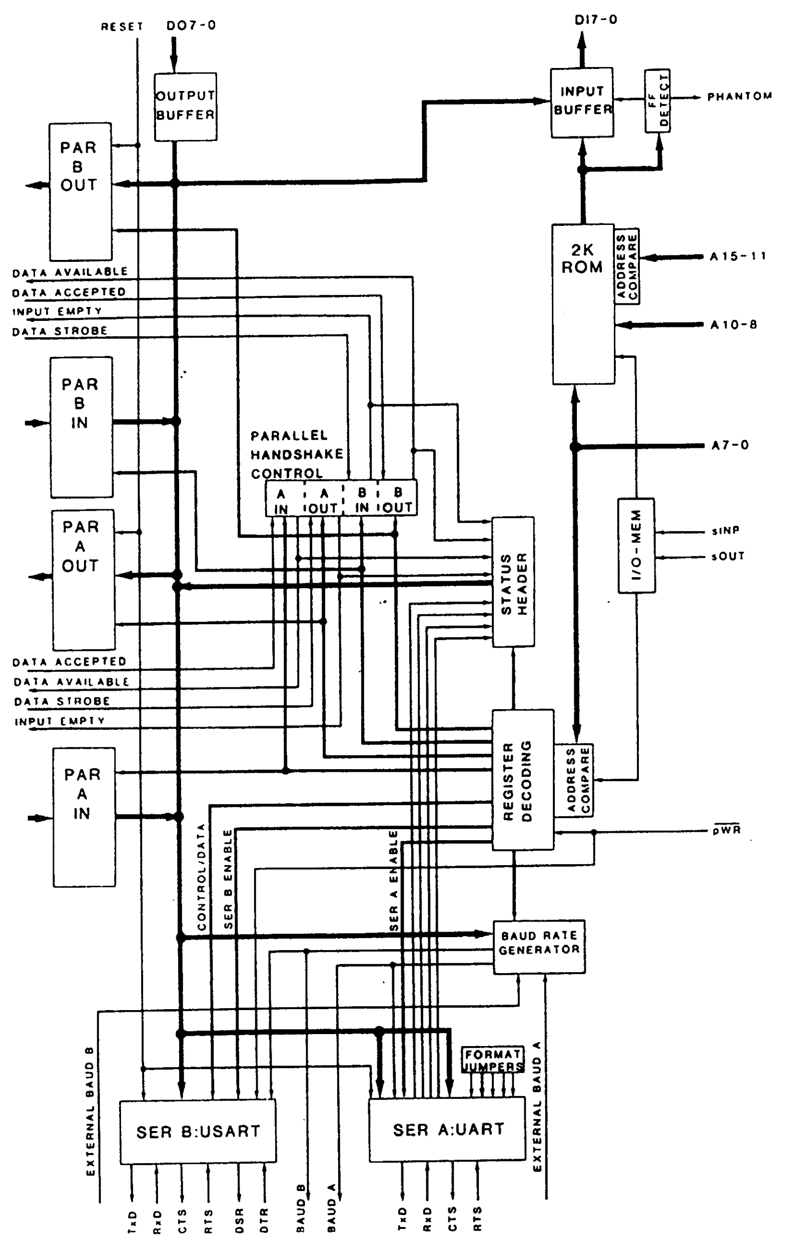
TABLE 1.3

When either SUP or PUP is high and I/O is high, OUTPUT ENABLE* goes low, enabling the Output Data Buffer, which gates data from the S-100 bus. OUTPUT ENABLE* high tri-states the Output Data Buffer.

PUP high forces SUP low, allowing the parallel ports to overlay one of the serial ports. If the parallel ports overlay the USART, parallel status information will still be available at the UART status address. This is accomplished when PAR ADDR 2-7 and SER ADDR 2-7 are set to the same value and PAR ADDR 1 is set to 1 (or 0 if A1 is inverted by SPR).

FIGURE 1.1

2718 BLOCK DIAGRAM



1.2 PARALLEL PORTS

The 2718's two parallel ports provide bi-directional 8-bit interfacing with four-line handshaking. Each parallel port consists of separate buffered input and output registers. The Parallel Port Decoder decodes A0 and sOUT to activate one of the four register-enabling lines PAR*, PAW*, PBR*, and PBW* (Parallel A and B Read and Write). The input buffers are permanently enabled, while the output buffers can be enabled by the peripheral device or constantly enabled (see Section 2.1.9).

The register latches are controlled by the register-enable lines and the handshake inputs. DATA STROBE, by which the peripheral indicates that it has made valid data available, gates data into the Input Latch and clears the Input Status Flip-Flop to indicate that the port has data to be read; PAR*/PBR* enables Input Latch output to the 2718's internal data bus, from which it is gated to the processor through the Input Data Buffer by pDBIN active, and sets the Input Status Flip-Flop to indicate INPUT EMPTY. The Output Latches operate similarly. PAW*/PBW* clocks data into the latch and clears the Output Status Flip-Flop to indicate DATA AVAILABLE; when the peripheral toggles DATA ACCEPTED, the Output Status Flip-Flop is reset. If jumper PAOE/PBOE is set to X (External), data will be available to the peripheral only when it pulls pin 5 or pin 6 low (see Section 2.1.9). The Output Registers are cleared by EXT CLR* low. The Status Flip-Flop outputs INPUT EMPTY A and B and DATA AVAILABLE A and B are also the parallel port status bits.

1.3 SERIAL PORTS

Because peripheral equipment that communicates serially can do so in a variety of formats, the 2718 incorporates two different serial interface chips: a Universal Asynchronous Receiver/Transmitter (UART), and a Universal Synchronous/Asynchronous Receiver/Transmitter (USART). Together these chips allow interfacing with a wide variety of serial devices. A general description of their implementation in the 2718 follows. For a table of UART and USART inputs and outputs and a discussion of the internal operation of the chips, see Appendix B.

1.3.1 SERIAL PORT A: THE UART

The UART translates parallel data to asynchronous serial data and vice versa according to jumper-determined format inputs (see Section 2.1.11). When transmitting, it arranges the parallel data serially in a 5- to 8-bit word, adds a start bit, a parity bit if parity is enabled, and 1, 1½, or 2 stop bits, then shifts the data onto TxD. When receiving, the UART strips the start and stop bits, checks parity if enabled, makes the data available in parallel on the 2718's internal data bus, and provides format error and status information. UART transmitting and receiving are controlled by the SAR* and SAW* (Serial A Read and Write) outputs of the Serial A decoder. A low on EXT CLR*, inverted, resets the UART.

1.3.2 SERIAL PORT B: THE USART

The USART is enabled by SBS* (Serial B Select*) when addressed. Command words program the USART to the mode and format desired, C/D* (controlled by A0) high and WR* (controlled by pWR*) low selecting the command register; the commands themselves are given in Section 3.3. When mode and format have been programmed, a low on C/D* enables data transmitting (pWR* low) or receiving (pWR* high). Like the UART, the USART is reset by EXT CLR* low inverted high.

1.3.3 BAUD RATE GENERATION

The serial port data transfer rates are controlled by BAUDA and BAUDB. Two sets of jumpers allow hardwiring or software-selection of the desired baud rates. If the software mode is selected, the baud rate byte, clocked into the Baud Rate Register by WBAUD*, is input to the Baud Rate Select Multiplexer. If the jumpers are set for the hardware mode, the mux inputs are determined solely by the jumper positions, no matter what is written to the Baud Rate Latch.

A 4702 programmable bit rate generator provides thirteen different baud rates. In addition, a multiplexed input (IM) allows externally-generated baud rates (input from the peripherals along with the handshake lines) to be output by the 4702. Multiplexer U32 provides either a 19.2K baud rate or multiplexed ExtA and ExtB baud rates for input through IM. The output of the 4702 reflects the multiplexing of the inputs. Two AND gates, an inverter, and two flip-flops form a two-bit addressable latch which demultiplexes the output into the separate signals BAUDA and BAUDB.

1.4 STATUS REGISTERS

The 2718 has two status registers. One is addressed at Serial Port B as shown in Table 1.3, and is internal to the USART. The other, addressed at Serial Port A as shown in Table 1.2, consists of four bits each of UART and Parallel Port status. The UART status bits are described in Section 3.2; the Parallel Ports' status bits reflect their handshake outputs INPUT EMPTY and DATA AVAILABLE. Enhancing the flexibility of the 2718, the Status Select Header allows user formatting of the Ser A/Par status register. This permits emulation of other boards, providing compatibility with pre-existing software.

1.5 CONTROL ROM

Provision is made on-board the 2718 for a 2K EPROM, in which may be stored the peripheral driver programs. Driver software must be supplied by the user; see Chapter 4 for examples. If the driver routines are to be stored elsewhere in the system, the 2718's ROM socket may be used for 2K of general purpose ROM, or may be left empty, in which case it will occupy no memory space. FF Detect Circuitry allows programming of the EPROM on a byte-by-byte basis. The open collector output of the NANDing of the data lines (FFD*) is pulled low when the internal data bus lines are all 1's (FFh); FFD* low disables the Input Data Buffer. Thus 2718 ROM locations will not conflict with other memory locations having the same addresses if the 2718 locations are left in the unprogrammed (all 1's) state.

The ROM is enabled when both PRUP (PROM Up) and MEM/IO* are high. PRUP is high when ROM ADDR jumpers 15-11 match address bits A15-A11, allowing location of the ROM at any 2K boundary within 64K. ROM output is enabled only when pWR* is high. Phantom Circuitry allows the 2718 ROM to overlay other system memory that is disabled by PHANTOM*. For example, if on-board 2718 driver routines are used with a CCS 2810 CPU, the ROM base address should be set to F000h and the PHNTM jumper should be set to E. When an address common to the Monitor and a routine on the 2718 ROM is put on the address bus, the 2718 pulls PHANTOM* low to disable the CPU ROM. The 2718 ROM retains control until an unprogrammed location is addressed, a jump out of the routine is executed, or the top address on the ROM has been read. When an empty location is addressed, the low on FFD* forces PHANTOM* high, allowing program control to default to the Monitor ROM.

CHAPTER 2

SET-UP

2.1 JUMPERS

A number of features on the 2718 must be jumper-configured. Figure 2.1 shows the locations of the jumpers on the board. To set a jumper, firmly seat a blue Berg jumper plug over the two header pins corresponding to the desired setting.

2.1.1 PARA ADDR 1-7, SER ADDR 2-7

The seven most significant bits of the parallel ports' base address are set on the PAR ADDR jumpers. The six most significant bits of the serial ports' base address are set on the SER ADDR jumpers. Jumper 7 sets the most significant bit in each case. Table 2.1 gives the binary form of all possible port addresses.

2.1.2 SPR

The Serial Ports Reverse jumper inverts the A1 signal that enables either the Serial A or Serial B port. When the SPR jumper is set to N (non-inverted), SER A is selected by a A1=0 and SER B by A1=1. Setting the SPR jumper to I (inverted) causes SER A to be selected by A1=1 and SER B by A1=0. See Figure 2.2.

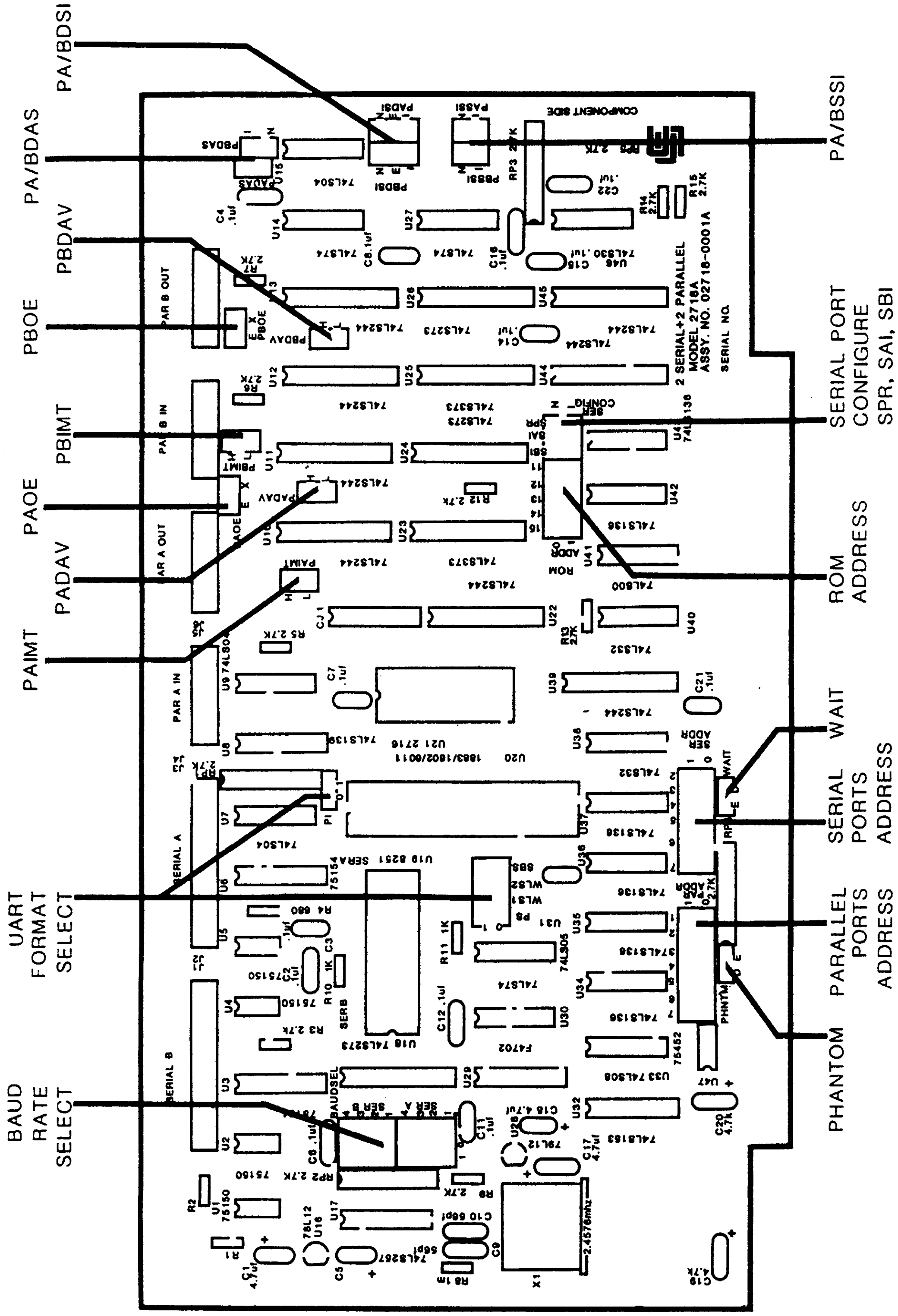
TABLE 2.1

POSSIBLE PORT ADDRESSES

ADDRESS BITS							PORT ADDRESS	
A7	A6	A5	A4	A3	A2	A1*	HEX	DECI
0	0	0	0	0	0	0	00	0
0	0	0	0	0	0	1	02	2
0	0	0	0	0	1	0	04	4
0	0	0	0	0	1	1	06	6
0	0	0	0	1	0	0	08	8
0	0	0	0	1	0	1	0A	10
0	0	0	0	1	1	0	0C	12
0	0	0	0	1	1	1	0E	14
0	0	0	1	0	0	0	10	16
0	0	0	1	0	0	1	12	18
0	0	0	1	0	1	0	14	20
0	0	0	1	0	1	1	16	22
0	0	0	1	1	0	0	18	24
0	0	0	1	1	0	1	1A	26
0	0	0	1	1	1	0	1C	28
0	0	0	1	1	1	1	1E	30
0	0	1	0	0	0	0	20	32
0	0	1	0	0	0	1	22	34
0	0	1	0	0	1	0	24	36
0	0	1	0	0	1	1	26	38
0	0	1	0	1	0	0	28	40
0	0	1	0	1	0	1	2A	42
0	0	1	0	1	1	0	2C	44
0	0	1	0	1	1	1	2E	46
0	0	1	1	0	0	0	30	48
0	0	1	1	0	0	1	32	50
0	0	1	1	0	1	0	34	52
0	0	1	1	0	1	1	36	54
0	0	1	1	1	0	0	38	56
0	0	1	1	1	0	1	3A	58
0	0	1	1	1	1	0	3C	60
0	0	1	1	1	1	1	3E	62
0	1	0	0	0	0	0	40	64
0	1	0	0	0	0	1	42	66
0	1	0	0	0	1	0	44	68
0	1	0	0	0	1	1	46	70
0	1	0	0	1	0	0	48	72
0	1	0	0	1	0	1	4A	74
0	1	0	0	1	1	0	4C	76
0	1	0	0	1	1	1	4E	78
0	1	0	1	0	0	0	50	80
0	1	0	1	0	0	1	52	82
0	1	0	1	0	1	0	54	84
0	1	0	1	0	1	1	56	86
0	1	0	1	1	0	0	58	88
0	1	0	1	1	0	1	5A	90
0	1	0	1	1	1	0	5C	92
0	1	0	1	1	1	1	5E	94
0	1	1	0	0	0	0	60	96
0	1	1	0	0	0	1	62	98
0	1	1	0	0	1	0	64	100
0	1	1	0	0	1	1	66	102
0	1	1	0	1	0	0	68	104
0	1	1	0	1	0	1	6A	106
0	1	1	0	1	1	0	6C	108
0	1	1	0	1	1	1	6E	110
0	1	1	1	0	0	0	70	112
0	1	1	1	0	0	1	72	114
0	1	1	1	0	1	0	74	116
0	1	1	1	0	1	1	76	118
0	1	1	1	1	0	0	78	120
0	1	1	1	1	0	1	7A	122
0	1	1	1	1	1	0	7C	124
0	1	1	1	1	1	1	7E	126

*A1 of Serial Ports' Base Address must equal 0.

ADDRESS BITS							PORT ADDRESS	
A7	A6	A5	A4	A3	A2	A1	HEX	DECI
1	0	0	0	0	0	0	80	128
1	0	0	0	0	0	1	82	130
1	0	0	0	0	1	0	84	132
1	0	0	0	0	1	1	86	134
1	0	0	0	1	0	0	88	136
1	0	0	0	1	0	1	8A	138
1	0	0	0	1	1	0	8C	140
1	0	0	0	1	1	1	8E	142
1	0	0	1	0	0	0	90	144
1	0	0	1	0	0	1	92	146
1	0	0	1	0	1	0	94	148
1	0	0	1	0	1	1	96	150
1	0	0	1	1	0	0	98	152
1	0	0	1	1	0	1	9A	154
1	0	0	1	1	1	0	9C	156
1	0	0	1	1	1	1	9E	158
1	0	1	0	0	0	0	A0	160
1	0	1	0	0	0	1	A2	162
1	0	1	0	0	1	0	A4	164
1	0	1	0	0	1	1	A6	166
1	0	1	0	1	0	0	A8	168
1	0	1	0	1	0	1	AA	170
1	0	1	0	1	1	0	AC	172
1	0	1	0	1	1	1	AE	174
1	0	1	1	0	0	0	B0	176
1	0	1	1	0	0	1	B2	178
1	0	1	1	0	1	0	B4	180
1	0	1	1	0	1	1	B6	182
1	0	1	1	1	0	0	B8	184
1	0	1	1	1	0	1	BA	186
1	0	1	1	1	1	0	BC	188
1	0	1	1	1	1	1	BE	190
1	1	0	0	0	0	0	C0	192
1	1	0	0	0	0	1	C2	194
1	1	0	0	0	1	0	C4	196
1	1	0	0	0	1	1	C6	198
1	1	0	0	1	0	0	C8	200
1	1	0	0	1	0	1	CA	202
1	1	0	0	1	1	0	CC	204
1	1	0	0	1	1	1	CE	206
1	1	0	1	0	0	0	D0	208
1	1	0	1	0	0	1	D2	210
1	1	0	1	0	1	0	D4	212
1	1	0	1	0	1	1	D6	214
1	1	0	1	1	0	0	D8	216
1	1	0	1	1	0	1	DA	218
1	1	0	1	1	1	0	DC	220
1	1	0	1	1	1	1	DE	222
1	1	1	0	0	0	0	E0	224
1	1	1	0	0	0	1	E2	226
1	1	1	0	0	1	0	E4	228
1	1	1	0	0	1	1	E6	230
1	1	1	0	1	0	0	E8	232
1	1	1	0	1	0	1	EA	234
1	1	1	0	1	1	0	EC	236
1	1	1	0	1	1	1	EE	238
1	1	1	1	0	0	0	F0	240
1	1	1	1	0	0	1	F2	242
1	1	1	1	0	1	0	F4	244
1	1	1	1	0	1	1	F6	246
1	1	1	1	1	0	0	F8	248
1	1	1	1	1	0	1	FA	250
1	1	1	1	1	1	0	FC	252
1	1	1	1	1	1	1	FE	254

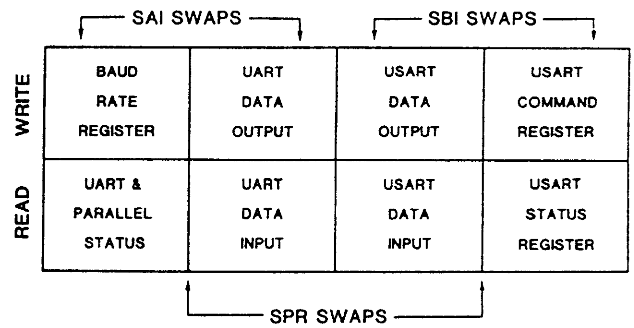


2718 JUMPER POSITIONS

FIGURE 2.1

2.1.3 SAI, SBI

FIGURE 2.2



The Serial A Invert jumper inverts the A0 signal that selects between the data and baud-rate/status registers of the UART. The data registers are selected by A0=1 when the SAI jumper is set to N, and by A0=0 when the jumper is set to I.

The Serial B Invert jumper similarly swaps the addresses of the command and data registers of the USART. The data registers are addressed by A0=1 when the SBI jumper is set to N, and by A0=0 when the jumper is set to I. The effects of SAI and SBI are shown in Figure 2.2.

2.1.4 PADSI, PBDSI

The Parallel A and B Data Strobe Invert jumpers control the polarity of the peripheral-generated DATA STROBE signals used to gate the Parallel Port Input Latches. Output follows input when the gate input (G) is high; output is latched by G going low. To latch data on the trailing edge of DATA STROBE, set a jumper to N if the signal is active high and to I if it is active low. The E position enables constant data flow (no latching) by holding G permanently high.

2.1.5 PASSI, PBSSI

STROBE ACTIVE	PxSSI SET TO	CLEAR WHEN STROBE IS
LOW	N	ACTIVE
LOW	I	INACTIVE
HIGH	N	INACTIVE
HIGH	I	ACTIVE

STATUS STROBE INVERT JUMPERS

TABLE 2.2

A read to a parallel port (PAR* or PBR* low) sets the port's Input Status Flip-Flop to indicate that data has been taken. The Parallel A and B Status Strobe Invert jumpers control the polarity of the DATA STROBE signals used to clear the Input Status Flip-Flops, which indicates that new data is available. If DATA STROBE is active high, set the SSI jumper to I; if it is active low, set the jumper to N.

2.1.6 PAIMT, PBIMT

The Parallel A and B Input Empty jumpers determine the sense polarity of the Input Empty handshake outputs. A setting of H produces a high-active signal; L produces a low-active signal.

2.1.7 PADAS, PBDAS

A write to a parallel port (PAW* or PBW* low) clears that port's Output Status Flip-Flop. The Parallel A and B Data Accepted Strobe jumpers reverse the polarity of the DATA ACCEPTED handshake signals used to clear the Output Status flip-flops. Thus a flip-flop is cleared when DATA ACCEPTED goes low if its jumper is set to N, and when DATA ACCEPTED goes high if its jumper is set to I.

2.1.8 PADAV, PBDAV

The Parallel A and B Data Available jumpers determine the polarity of the DATA AVAILABLE handshake outputs, which signify that new data is available to the peripheral device. Setting a jumper to H produces a high-active signal; L produces a low-active signal.

2.1.9 PAOE, PBOE

The Parallel A and B Output Enable jumpers allow external enabling of the parallel port output buffers. If a jumper is set to X, that port's output buffer will be enabled by a low to pin 5 or pin 6 of the output connector. If a jumper is set to E, the buffer's -Enable input is tied to ground and the buffer is constantly enabled.

2.1.10 UART FORMAT JUMPERS

TABLE 2.3

WLS 2	WLS 1	WORD LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

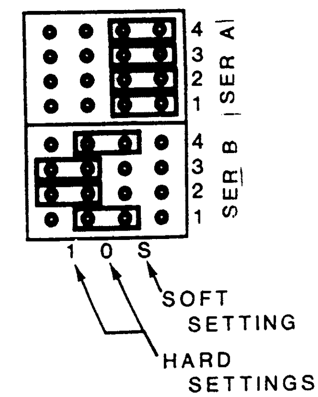
WORD LENGTH JUMPERS

These five jumpers control the format of serial data transfer by the UART. WLS 1 and 2 select the word length as indicated in Table 2.3. SBS selects the number of stop bits, a 0 selecting 1 stop bit and a 1 selecting 2 (1½ for 5-bit words). PI=1 inhibits parity generation/reading. If parity is not inhibited, PS=1 selects even parity, and PS=0 selects odd.

2.1.11 BAUD SEL

FIGURE 2.3.

BAUD SEL JUMPERS



The Baud Rate Select jumpers determine the rates of data transfer by the serial ports. The UART's transmitter and receiver clocks are supplied by BAUD A, while BAUD B serves as the clocks for the USART. The baud rate for each port is determined by a four-bit code. If the BAUD SEL jumpers for a port are set to S, the code is input through software. Jumper positions 1 and 0 allow the code to be hard-wired. The low-order bit of code, S0, is set on the #1 jumper, the high-order bit on #4. Figure 2.3 shows Serial Port A set for software control and Serial Port B set for 600 baud. The baud rate codes are given in Table 2.4.

TABLE 2.4

BAUD RATE CODES

S3	S2	S1	S0	BAUD RATE
0	0	0	0	19200
0	0	0	1	EXT
0	0	1	0	50
0	0	1	1	75
0	1	0	0	134.5
0	1	0	1	200
0	1	1	0	600
0	1	1	1	2400
1	0	0	0	9600
1	0	0	1	4800
1	0	1	0	1800
1	0	1	1	1200
1	1	0	0	2400
1	1	0	1	300
1	1	1	0	150
1	1	1	1	110

2.1.12 ROM ADDR

The five most significant bits of the base address of the on-board ROM are set on ROM ADDR jumpers 15-11. A15-A11 determine a 2K block; A10-A0 address a specific location in the block. Table 2.5 gives the jumper settings for each 2K block.

ROM ADDRESS TABLE

ADDRESS BITS					ROM ADDRESS	
A15	A14	A13	A12	A11	K=1024	HEX
0	0	0	0	0	0K	0000
0	0	0	0	1	2K	0800
0	0	0	1	0	4K	1000
0	0	0	1	1	6K	1800
0	0	1	0	0	8K	2000
0	0	1	0	1	10K	2800
0	0	1	1	0	12K	3000
0	0	1	1	1	14K	3800
0	1	0	0	0	16K	4000
0	1	0	0	1	18K	4800
0	1	0	1	0	20K	5000
0	1	0	1	1	22K	5800
0	1	1	0	0	24K	6000
0	1	1	0	1	26K	6800
0	1	1	1	0	28K	7000
0	1	1	1	1	30K	7800
1	0	0	0	0	32K	8000
1	0	0	0	1	34K	8800
1	0	0	1	0	36K	9000
1	0	0	1	1	38K	9800
1	0	1	0	0	40K	A000
1	0	1	0	1	42K	A800
1	0	1	1	0	44K	B000
1	0	1	1	1	46K	B800
1	1	0	0	0	48K	C000
1	1	0	0	1	50K	C800
1	1	0	1	0	52K	D000
1	1	0	1	1	54K	D800
1	1	1	0	0	56K	E000
1	1	1	0	1	58K	E800
1	1	1	1	0	60K	F000
1	1	1	1	1	62K	F800

TABLE 2.5

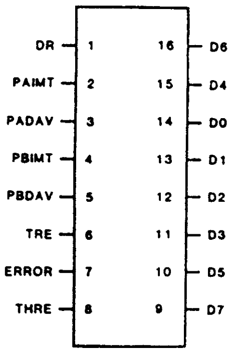
2.1.13 PHNTM

The PHANTOM* line allows routines in the on-board ROM to overlay your monitor or other memory which is disabled by PHANTOM* low. To enable the 2718's Phantom overlay capability, set the Phantom jumper to E. If the PHANTOM* line is not needed, disable it by setting the jumper to D.

2.1.14 WAIT

The processor samples pRDY in T2 of each instruction cycle and, if pRDY is low, inserts a wait state. The 2718 initiates a wait state, if the Wait jumper is set to E, in each cycle in which the board is active by pulling pRDY low when both pSYNC and FFD* (FF Detect: see Section 1.5) are high. Because the 2718 data bus is held high when inactive, qualifying pSYNC with FFD* allows wait state generation only when the 2718 is active. No wait states are initiated by the 2718 if the Wait jumper is set to D. Whether or not wait states will be necessary depends on the ROM and CPU speeds involved; the I/O devices do not require wait states.

2.2 STATUS HEADER



SERIAL A STATUS HEADER

FIGURE 2.4

The Ser A/Par Status Header allows the user to format the Serial A/Parallel status byte. Fig. 2.4 shows header inputs and outputs by pin number. Fig. 2.5 illustrates a sample configuration in which UART status bits DR and THRE emulate USART status bits 1 (RxRDY) and 0 (TxRDY), Parallel Port A status is in bits 2-3, Parallel Port B status is in bits 4-5, and UART status bits TRE and ERROR are not made available.

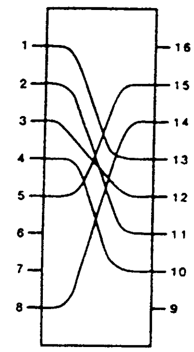


FIGURE 2.5

2.3 BUFFER POLARITY OPTION

The Parallel Port Input and Output Buffers, the System Bus Input and Output Buffers, the Address Buffer, and the Ser A/Par Status Buffer are non-inverting 74LS244's. Users who wish to invert any address, data, or status byte may do so by replacing the appropriate non-inverting buffer with a 74LS240 inverting buffer.

2.4 CABLE CONSTRUCTION

Because peripherals compatible with the 2718 use a wide variety of connector configurations, no cables are included with the board. Each parallel port requires a cable with a polarized female 14-pin connector (T&B/Ansley 6Ø9-14Ø3, AMP 88389-2) at the 2718 end and the appropriate connector at the mainframe end. Each serial cable requires a polarized female 26-pin connector (T&B/Ansley 6Ø9-26Ø3,or AMP 88423-5) at the 2718 end and usually a female DB-25S connector at the mainframe end. A 9-inch and an 18-inch serial cable are available separately from CCS (Products 7325A and 2ØØØA). A parallel cable will be offered soon; the product number is not available as of this writing, however.

Please note that the Serial Port B connector is at the far left of the board (J1), and that the Serial Port A connector is the next connector to the right (J2). Sections A.7 and A.8 show the parallel and serial connector pinouts.

CHAPTER 3

PROGRAMMING INFORMATION

This chapter gives the 2718 register formats and discusses UART and USART programming. The actual addresses of the registers depend on the settings of several jumpers. Section 1.1 discusses how the various registers are addressed, while Sections 2.1.1-2.1.3 deal with the jumpers involved. Table 3.1 on page 3-3 shows the relative addresses of the serial port registers for all possible combinations of SPR, SAI, and SBI jumpers.

3.1 PARALLEL PORTS

Parallel data transfer and handshaking are initiated by a read or write to a parallel port address; no other handshaking control is needed. Parallel port status can be read from the Serial Port A status register. Four status bits are available:

PAIMT, PBIMT } reflect the INPUT EMPTY handshake outputs.

PADAV, PBDAV } reflect the DATA AVAILABLE handshake outputs.

3.2 SERIAL PORT A

UART data transfer is initialized by a write to or read from a Serial Port A data register. All necessary handshaking is generated by the UART. Status can be read from the Serial A status register. There are four Serial A status bits:

TRE	TRANSMITTER REGISTER EMPTY = 1 indicates that the TxR is empty.
DR	DATA RECEIVED = 1 indicates that data has been received and transferred to the RxHR.
THRE	TRANSMITTER HOLDING REGISTER EMPTY, the result of the ANDing of the RTS handshake from the peripheral and the THRE output of the UART, indicates when set that a character may be loaded into the UART for transmission.
ERROR	ERROR = 1 indicates that no parity, overrun, or framing error has occurred.

3.3 SERIAL PORT B

The USART is initialized by 2, 3, or 4 control words written to the command register. The Mode Word comes first. It is followed by the Command Word if the asynchronous mode is selected. If the synchronous mode is selected, one or two Sync Words will separate the Mode Word and the Command Word. After a reset, which puts the USART in an idle state and clears its registers, the USART must be reinitialized.

The Mode Word has one of the following formats, depending on whether the synchronous or asynchronous mode is selected:

# SYNC CHARS	SYNDET IN/OUT	PARITY MODE	PARITY ENABLE	WORD LENGTH		MUST BE 00	
7	6	5	4	3	2	1	0

SYNC CONTROL WORD FORMAT

FIGURE 3.1

TABLE 3.1. JUMPER-DETERMINED SERIAL REGISTER ADDRESSES

REGISTER ADDRESSED	JUMPER SETTINGS							
	SPR=N SAI=N SBI=N	SPR=N SAI=N SBI=I	SPR=N SAI=I SBI=N	SPR=N SAI=I SBI=I	SPR=I SAI=N SBI=N	SPR=I SAI=N SBI=I	SPR=I SAI=I SBI=N	SPR=I SAI=I SBI=I
BAUD RATE	BASE WRITE	BASE WRITE	BASE+1 WRITE	BASE+1 WRITE	BASE+2 WRITE	BASE+3 WRITE	BASE+2 WRITE	BASE+3 WRITE
SER A/PAR STATUS	BASE READ	BASE READ	BASE+1 READ	BASE+1 READ	BASE+2 READ	BASE+3 READ	BASE+2 READ	BASE+3 READ
SERIAL A DATA OUT	BASE+1 WRITE	BASE+1 WRITE	BASE WRITE	BASE WRITE	BASE+3 WRITE	BASE+2 WRITE	BASE+3 WRITE	BASE+2 WRITE
SERIAL A DATA IN	BASE+1 READ	BASE+1 READ	BASE READ	BASE READ	BASE+3 READ	BASE+2 READ	BASE+3 READ	BASE+2 READ
SERIAL B COMMAND	BASE+2 WRITE	BASE+3 WRITE	BASE+2 WRITE	BASE+3 WRITE	BASE WRITE	BASE WRITE	BASE+1 WRITE	BASE+1 WRITE
SERIAL B STATUS	BASE+2 READ	BASE+3 READ	BASE+2 READ	BASE+3 READ	BASE READ	BASE READ	BASE+1 READ	BASE+1 READ
SERIAL B DATA OUT	BASE+3 WRITE	BASE+2 WRITE	BASE+3 WRITE	BASE+2 WRITE	BASE+1 WRITE	BASE+1 WRITE	BASE WRITE	BASE WRITE
SERIAL B DATA IN	BASE+3 READ	BASE+2 READ	BASE+3 READ	BASE+2 READ	BASE+1 READ	BASE+1 READ	BASE READ	BASE READ

BITS 1,0 — 00 = synchronous mode

BITS 3,2 — 00 = 5 bits per character
01 = 6 bits per character
10 = 7 bits per character
11 = 8 bits per character

BIT 4 — 0 = disable parity
1 = enable parity

BIT 5 — 0 = odd parity
1 = even parity

BIT 6 — 0 = SYNDET, pin 16, output
1 = SYNDET input
(Please note that because the 2718 does not use pin 16, this bit must always be programmed to 0.)

BIT 7 — 0 = two SYNC characters
1 = one SYNC character

---

* STOP BITS		PARITY MODE	PARITY ENABLE	WORD LENGTH		NOT 00: BAUD RATE FACTOR	
7	6	5	4	3	2	1	0

ASYNC CONTROL WORD FORMAT

FIGURE 3.2

BITS 1,0 — 01 = asynchronous, 1 x baud rate
10 = asynchronous, 16 x baud rate
11 = asynchronous, 64 x baud rate

BITS 3,2 — 00 = 5 bits per character
01 = 6 bits per character
10 = 7 bits per character
11 = 8 bits per character

BIT 4 — 0 = disable parity
1 = enable parity

BIT 5 — 0 = odd parity
1 = even parity

BITS 7,6 — 00 invalid
01 = 1 stop bit
10 = 1.5 stop bits
11 = 2 stop bits

If the synchronous mode has been selected, the Mode Word is followed by one or two sync characters (as specified by bit 7 of the Mode Word). These characters must precede all data transmitted or received by the USART.

The Command Word initiates specific USART functions, such as resetting flags and searching for sync characters. Commands may be issued at any point in a program by a write to the USART's command address. Command Words have the following format:

EH	IR	CTS	ER	SBRK	RxEN	DSR	TxEN
7	6	5	4	3	2	1	0

COMMAND WORD FORMAT

FIGURE 3.3

TxEN — TRANSMITTER ENABLE must be 1 for transmission to be enabled.

DSR — DATA SET READY = 1 forces the DSR handshake line high.

RxEN — RECEIVER ENABLE = 1 enables RxRDY output, pin 14, which is NOT USED BY THE 2718. When RxE is low, the OE flag is usually set; therefore we recommend that RxE be programmed to 1.

SBRK — SEND BREAK = 1 forces TxD output low until a subsequent Command word resets SBRK.

ER — ERROR RESET = 1 clears the error flags.

CTS — CLEAR TO SEND determines the polarity of CTS; a 1 forces CTS to 1. CTS is used for handshaking only, and has no effect on the transmission of data.

IR — INTERNAL RESET = 1 forces the USART into the idle mode; re-initializing is required before any forther operation is performed.

EH — ENTER HUNT = 1 causes the receiver to search for the sync word(s). The Hunt mode continues until the sync characters are found, a Command is sent in which EH = 0, or the USART is reset (externally or by IR = 0). This bit does not affect asynchronous operation.

USART status can be read from the status register. The status byte has the following format:

DTR	SYNDET	FE	OE	PE	TxE	RxRDY	TxRDY
7	6	5	4	3	2	1	0

USART STATUS BYTE FORMAT

FIGURE 3.4

TxRDY	TRANSMITTER READY = 1 indicates that the Transmitter Holding Register is empty.
RxRDY	RECEIVER READY = 1 indicates that a character is present in the Receiver Holding Register.
TxE	TRANSMITTER EMPTY = 1 indicates that the Transmitter Register is empty.
PE	PARITY ERROR = 1 indicates an incorrect number of 1's in a received character.
OE	OVERRUN ERROR = 1 indicates that a character has been overwritten in the RxHR.
FE	FRAMING ERROR = 1 indicates that an improperly-formatted async character has been received in the RxHR.
SYNDET	SYNC DETECTION reflects synchronous mode control bit 6, indicating either internal or external synchronization. The 2718 uses internal sync; therefore the SYNDET bit should always be 0.
DTR	DATA TERMINAL READY is set by the DTR handshake signal to indicate that the peripheral is ready.

3.4 BAUD RATE

If the BAUDSEL jumpers for the UART and/or USART are set to S, the corresponding baud rate(s) are programmed by a write to Serial Port A's baud rate register, the low nibble of the baud rate byte determining the UART (Ser A) baud rate, the high nibble determining the USART (Ser B) baud rate, as illustrated in Figure 3.5. Table 3.1 gives the baud rate codes.

SER B BAUD RATE CODE				SER A BAUD RATE CODE			
S3	S2	S1	S0	S3	S2	S1	S0
7	6	5	4	3	2	1	0

BAUD RATE BYTE FORMAT

FIGURE 3.5

BAUD RATE CODES

4	3	2	1	BAUD RATE
0	0	0	0	19200
0	0	0	1	EXT
0	0	1	0	50
0	0	1	1	75
0	1	0	0	134.5
0	1	0	1	200
0	1	1	0	600
0	1	1	1	2400
1	0	0	0	9600
1	0	0	1	4800
1	0	1	0	1800
1	0	1	1	1200
1	1	0	0	2400
1	1	0	1	300
1	1	1	0	150
1	1	1	1	110

TABLE 3.1

3.8. SOFTWARE EXAMPLES

The following code sequences initialize and control Serial Port B of the 2718 as an interface for a Diablo Hi-Type printer. They may be used as is by owners of the CCS 2422 Disk Controller with CCS-modified CP/M, and as examples by those using other software.

```
        ;THIS CODE INITIALIZES PORT B (THE USART) OF THE 2718
        ;I/Ø BOARD FOR ASYNCHRONOUS, 8-BIT, NO-PARITY DATA
        ;TRANSFER.
        ;
ØØØØ AF         XRA     A       ;CLEAR A
ØØØ1 D3 Ø3      OUT     LISTS   ;ENSURE COMMAND MODE
ØØØ3 D3 Ø3      OUT     LISTS   ;
ØØØ5 D3 Ø3      OUT     LISTS   ;
ØØØ7 3E 4Ø      MVI     A,Ø4ØH  ;SOFTWARE RESET
ØØØ9 D3 Ø3      OUT     LISTS   ;
ØØØB 3E CE      MVI     A,ØCEH  ;MODE WORD IS 11ØØ111Ø
ØØØD D3 Ø3      OUT     LISTS   ;
ØØØF 3E 37      MVI     A,Ø37H  ;COMMAND WORD IS ØØ11Ø111
ØØ11 D3 Ø3      OUT     LISTS   ;
```

```
        ;LINE PRINTER DRIVER  FOR  CP/M  LIST DEVICE USING
        ;CCS  MODEL 2718   I/O  BOARD  AND  DATA  TERMINALS
        ;CORPORATION MODEL 300/S (DIABLO HITYPE 1).
        ;
        ;THIS  DRIVER  PROVIDES  A  SIMPLE  LST: INTERFACE
        ;TO  CCS'S  CCBIOS  PORTION  OF  CP/M VERSION 2.2,
        ;USING  PORT  B  (THE 8251  USART)  OF  THE  2718.
        ;THE DATA TERMINAL READY (DTR) SIGNAL ON  RS-232-C
        ;PIN 20  (REFLECTED BY BIT 7 OF THE USART'S STATUS
        ;REGISTER)  IS  HONORED  TO PREVENT OVERRUNNING OF
        ;THE PRINTER'S BUFFER.
        ;
        ;
        LIST:
1000 CD 5A F8   CALL    LPSTAT   ;RETRIEVE PRINTER PORT STATUS
1003 B7         ORA     A        ;SET THE ZERO FLAG ON STATUS
1004 CA 4F F8   JZ      LIST     ;LOOP ON BUSY STATUS
1007 79         MOV     A,C      ;PUT PASSED CHARACTER IN A
1008 D3 02      OUT     LISTD    ;OUTPUT CHARACTER TO PORT
100A C9         RET              ;RETURN TO CALLER
        ;
        ;
        ;THE  LPSTAT  ROUTINE  PROVIDES COMPATIBILITY WITH
        ;DIGITAL RESEARCH'S "DESPOOL" UTILITY AND COMPLIES
        ;WITH CP/M 2.2 CONVENTIONS.   IT  RETURNS  TO  THE
        ;CALLER WITH THE ACCUMULATOR EITHER RESET TO ZERO,
        ;IF THE PRINTER IS  BUSY,  OR SET TO 0FFH,  IF THE
        ;PRINTER IS READY TO ACCEPT ANOTHER CHARACTER.
        ;
        ;
        LPSTAT:
100B DB 03      IN      LISTS    ;INPUT PRINTER STATUS
100D E6 01      ANI     01H      ;MASK USART'S TxRDY BIT AND SET
                                 ;ZERO FLAG ON STATUS
100F C8         RZ               ;RETURN TO CALLER WITH ZERO FLAG
                                 ;SET IF Tx BUFFER FULL--ELSE,
1010 DB 03      IN      LISTS    ;INPUT PRINTER STATUS
1012 E6 80      ANI     080H     ;MASK OUT DTR BIT AND SET ZERO FLAG
1014 EE 80      XRI     080H     ;
1016 C9         RET              ;PASS STATUS BACK TO CALLER
```

APPENDIX A

TECHNICAL INFORMATION

A.1 SPECIFICATIONS

SIZE

Board: 10" l x 5" w
Connector: 6.35" l x .3" w (2.125" from right of board)
Component Ht: less than .5"

POWER SUPPLY

+8, +16, -16 Volts Regulated On-Board to +5, +12, -12 Volts

Consumption .75 Amps at +8 Volts
.05 Amps at +16 Volts
.05 Amps at -16 Volts

Heat Burden 110 gram-calories/minute
.45 BTU/minute

ENVIRONMENTAL REQUIREMENTS

Temperature: 0°C. to +70°C.
Humidity: up to 90%

INTERFACING

Parallel:
- Full Bi-Directional Handshaking
- TTL-Compatible Outputs
- Hardware-Programmable Data and Strobe Polarity
- Hardware-Programmable Status Bit Positions
- Jumper-Selectable Base Address

Serial:
- Meets RS-232-C Specifications
- Jumper-Selectable Base Address
- Standard Baud Rates from 75 to 19.2K Plus Externals
- Baud Rates Hardware- and/or Software-Programmable
- 1602 UART: Hardware-Programmable Status and Async Data Formats
- 8251 USART: Software-Programmable Sync/Async Data Formats

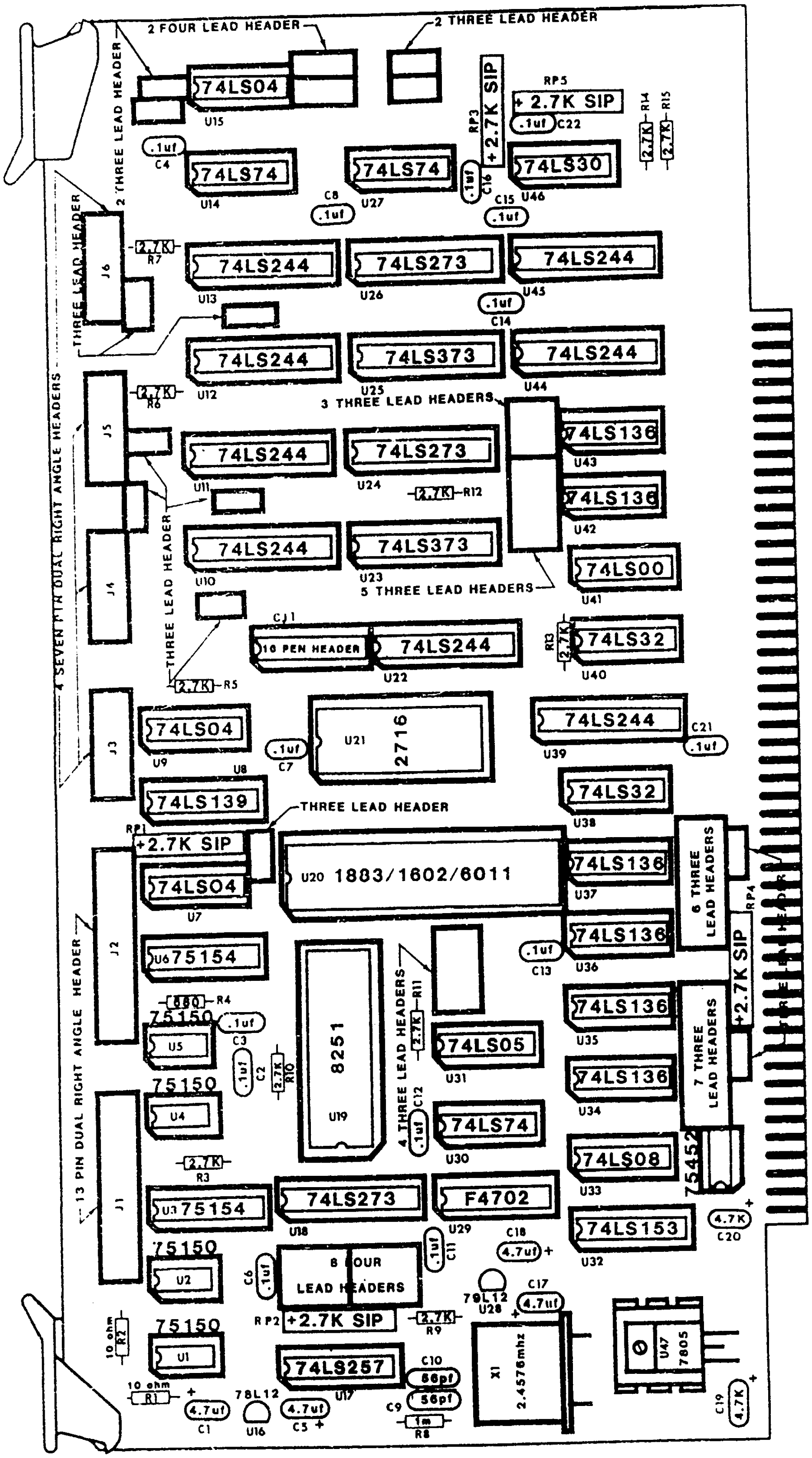
MEMORY

- Circuitry For 2716-Type 2K ROM
- Jumper-Selectable Base Address
- FF Detect for 1 Byte to 2K Byte Memory Size
- Jumper-Selectable Phantom Output
- Jumper-Selectable Wait State

ADDITIONAL FEATURES

- Reliable, easy-to-use Berg jumper plugs
- Low-power Schottky and MOS devices for minimum power consumption
- Sockets for all ICs
- Fiberglass epoxy (FR-4) PC board
- Solder-mask on both sides
- Gold-plated connector fingers
- Silk-screened component outlines, part designation, reference numbers

A.2 COMPONENT LAYOUT DIAGRAM



A.3 PARTS LIST

QTY	REF	DESCRIPTION	CCS PART #
Integrated Circuits			
4	U1-2,U4-5	75150 RS232C line drvr	30300-00150
2	U3,U6	75154 RS232C line rcvr	30300-00154
3	U7,U9,U15	74LS04 hex inverters	30000-00004
1	U8	74LS139 dual 2:4 decoder	30000-00139
8	U10-13,U22, U39,U44-55	74LS244 3-state octal buffers	30000-00244
3	U14,U27,U30	74LS74 dual D flip-flops	30000-00074
1	U16	78L12 +12v regulator	32000-17812
1	U17	74LS257 quad 3-state mux	30000-00257
3	U18,U24,U26	74LS273 octal d flip-flops	30000-00273
1	U19	8251 USART	31200-08251
1	U20	1602 UART	31200-01602
2	U23,U25	74LS373 octal D latches	30000-00373
1	U28	79L12 -12v regulator	32000-17912
1	U29	4702 prog bit rate generator	31000-04702
1	U31	74LS05 hex inverters, OC	30000-00005
1	U32	74LS153 dual 4:1 mux	30000-00153
1	U33	74LS08 quad 2-in AND	30000-00008
6	U34-37,U42-43	74LS136 quad EX-OR	30000-00136
2	U38,U40	74LS32 quad 2-in OR	30000-00032
1	U41	74LS00 quad 2-in NAND	30000-00000
1	U41	74LS30 8-in NAND	30000-00030
1	U47	7805 +5v regulator	32000-07805
1	U48	75452 dual periph NAND drvr	30300-00452
Capacitors			
6	C1,C5,C17-20	Tantalum, 4.7uf, 35v, 20%	42804-54756
14	C2-4,C6-8, C11-16,C21,C22	Mono, .1uf, 50v, 20%	42034-21046
2	C9,C10	Mica. 56pf, 500v, 10%	42215-55605

QTY	REF	DESCRIPTION	CCS PART #
Resistors			
2	R1,R2	10 ohm, 1/4 W, 5%	40002-01005
9	R3,R5-7, R9,R12-15	2.7K ohm, 1/4 W, 5%	40002-02725
1	R4	680 ohm, 1/4 W, 5%	40002-06815
1	R8	1 megohm, 1/4 W, 5%	40002-01055
2	R10,R11	1K ohm, 1/4 W, 5%	40002-01025
5	RP1-5	2.7K ohm x 7, SIP, 20%	40930-72726
Sockets			
5	XU1,2,4,5,48	8 pin	58102-00080
18	XU7,9,14,15, 27,30,31,33- 38,40-43,46	14 pin	58102-00140
7	XU3,6,8,17, 29,32,XCJ1	16 pin	58102-00160
13	XU10-13,18,22- 26,39,44,45	20 pin	58102-00200
1	XU21	24 pin	58102-00240
1	XU19	28 pin	58102-00280
1	XU20	40 pin	58102-00400
Miscellaneous			
1	X1	Crystal, 2.4576 mHz	48132-45762
1	CJ1	Header, 16 Pin	55000-10000
1	CJ1	Header Cover, 16 Pin	55000-10001
4	J3-6	Conn, 2 x 7, rt angle	55000-02070
2	J1,2	Conn, 2 x 13, rt angle	55000-02130
48		Conn, Molex, 1 x 3	56004-01003
10		Conn, Molex, 1 x 4	56004-01004
58		Berg jumper plugs	56200-00001
1	XU47	Heatsink, 220 .5" blk anodized	60022-00001
1		Screw, 6-32 x 5/16"	71006-32051
1		Nut, hex, KEP 6-32	73006-32001
2		Extractor, PCB, non-locking	60010-00001
2		Roll pin extractor mounting	60010-00000
1		PC Board, 2718, rev A	02718-00002

A.4 DEFINITION OF RS-232-C INTERFACE CONFIGURATION TYPES

A	Transmit Only
B	Transmit Only*
C	Receive Only
D	Half Duplex; or Duplex*
E	Full Duplex
F	Primary Channel Transmit Only* /Secondary Channel Receive Only
G	Primary Channel Receive Only / Secondary Channel Transmit Only*
H	Primary Channel Transmit Only / Secondary Channel Receive Only
I	Primary Channel Receive Only / Secondary Channel Transmit Only
J	Primary Channel Transmit Only* / Half Duplex Secondary Channel
K	Primary Channel Receive Only / Half Duplex Secondary Channel
L	Half Duplex Primary Channel / Half Duplex Secondary Channel; or
L	Duplex Primary Channel* / Duplex Secondary Channel*
M	Duplex Primary Channel / Duplex Secondary Channel
Z	Special (Circuits specified by supplier)

*Note the inclusion below of Request to Send in a Transmit Function, where it would not ordinarily be expected, but could indicate a non-transmit mode to the data communications equipment (DCE) to permit it to remove a line signal or to send synchronizing or framing signals as required.

A.5 STANDARD INTERFACE CONFIGURATIONS FOR RS-232-C

Interchange Circuit		Interface Configuration A	B	C	D	E	F	G	H	I	J	K	L	M	Z
AA	Protective Ground	-	-	-	-	-	-	-	-	-	-	-	-	-	-
AB	Signal Ground / Common Return	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BA	Transmitted Data	X	X		X	X	X		X		X		X	X	O
BB	Received Data			X	X	X		X		X		X	X	X	O
CA	Request to Send		X		X		X				X		X		O
CB	Clear to Send	X	X		X	X	X		X		X		X	X	O
CC	Data Set Ready	X	X	X	X	X	X	X	X	X	X	X	X	X	O
CD	Data Terminal Ready	S	S	S	S	S	S	S	S	S	S	S	S	S	O
CE	Ring Indicator	s	s	s	s	s	s	s	s	s	s	s	s	s	o
CF	Received Line Signal Detector			X	X	X		X		X		X	X	X	O
CG	Signal Quality Detector														o
CH/CI	Data Signalling Rate Selector (DTE/DCE)														o
DA/DB	Transmit Signal Element Timing (DTE/DCE)	T	T		T	T	T		T		T	T	T	T	O
DD	Receiver Signal Element Timing (DCE)			T	T	T		T		T		T	T	T	O
SBA	Secondary Transmitted Data							x		x	x	x	x	x	o
SBB	Secondary Received Data						x		x		x	x	x	x	o
SCA	Secondary Request to Send							x			x	x	x		o
SCB	Secondary Clear to Send							x		x	x	x	x	x	o
SCF	Secondary Received Line Signal Detector						x		x		x	x	x	x	o

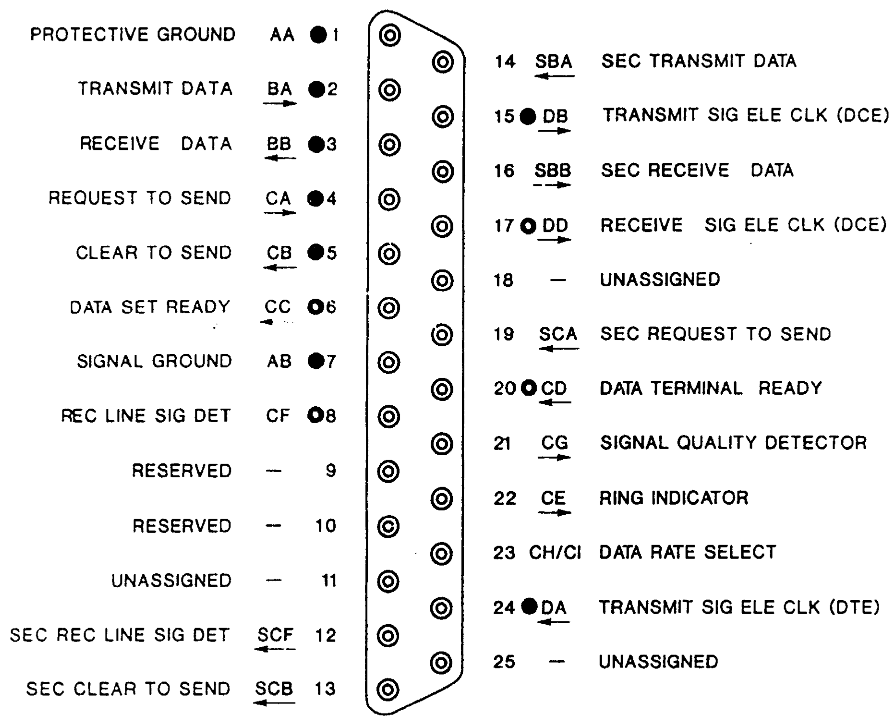
Notes:

Upper case indicates a line supported by the CCS 2718.
Lower case indicates a line not supported by the CCS 2718.

X = Basic interchange circuits, all systems
T = Additional interchange circuits required for synchronous channel
S = Additional interchange circuits required for switched service
O = Specified by supplier as required
- = Optional; supported by the CCS 2718

A.6 RS-232-C CONNECTOR PINOUT

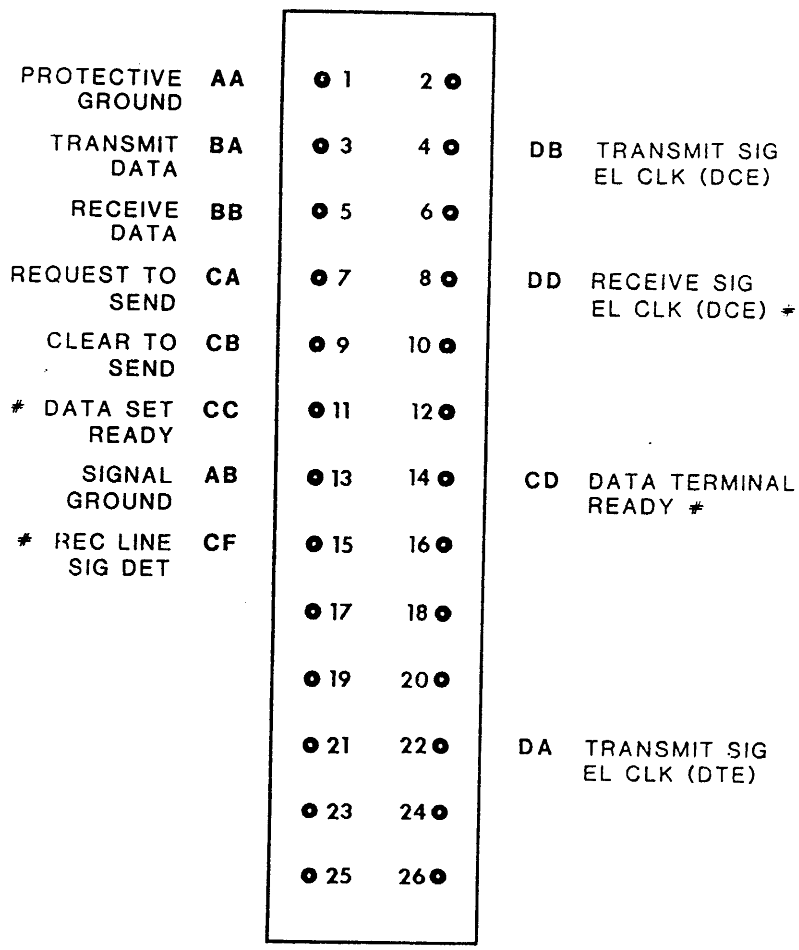
FRONT VIEW



DB-25S (FEMALE)

● Supported by Ports A and B.
○ Supported by Port B only.

A.7 SERIAL CONNECTOR PINOUTS



* Supported by Port B only.

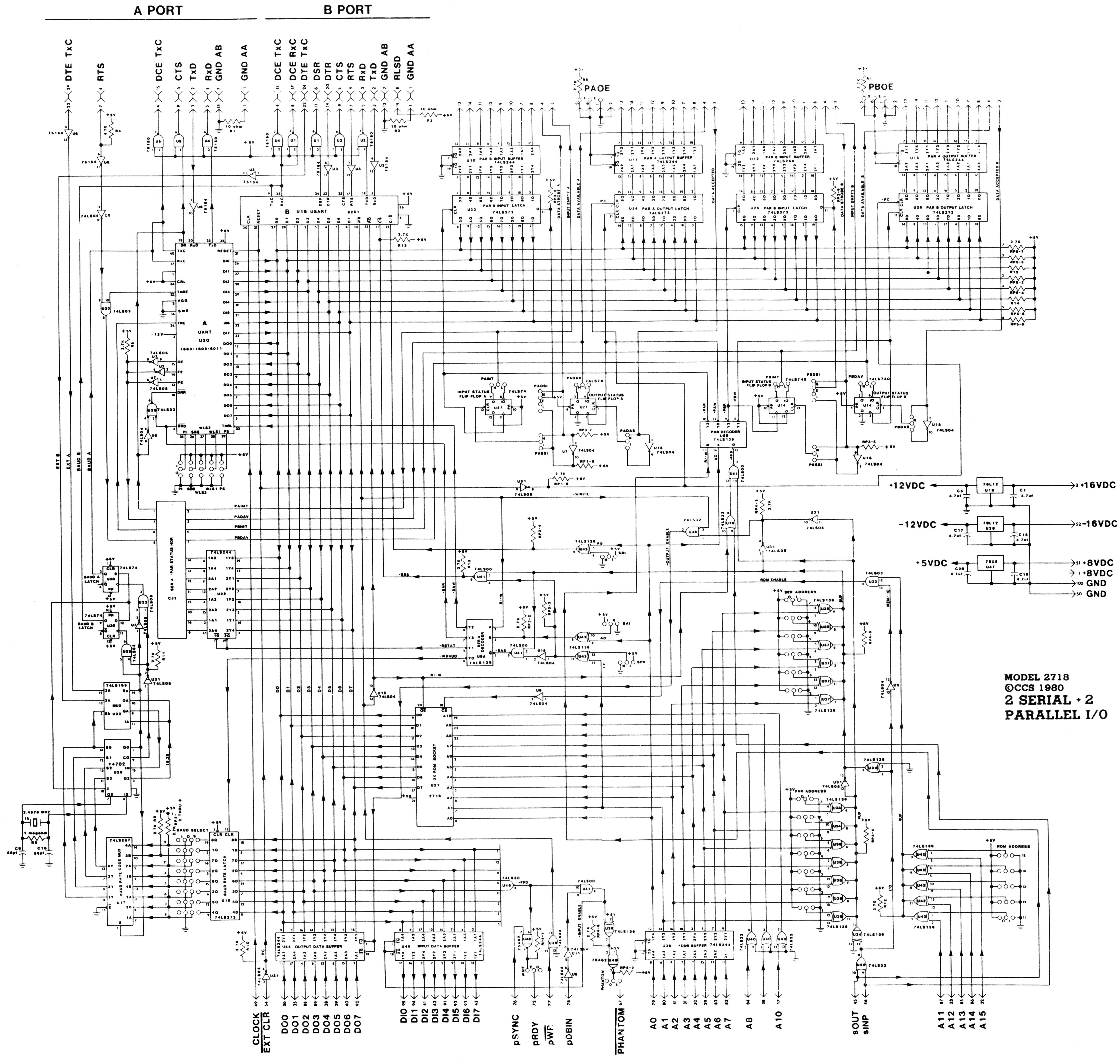
A.8 PARALLEL CONNECTOR PINOUTS

OUTPUT

GROUND	1	2	GROUND
DATA ACCEPTED	3	4	DATA AVAILABLE
ENABLE	5	6	ENABLE
D6	7	8	D7
D4	9	10	D5
D2	11	12	D3
D0	13	14	D1

INPUT

GROUND	1	2	GROUND
INPUT EMPTY	3	4	DATA STROBE
NOT USED	5	6	NOT USED
D6	7	8	D7
D4	9	10	D5
D2	11	12	D3
D0	13	14	D1

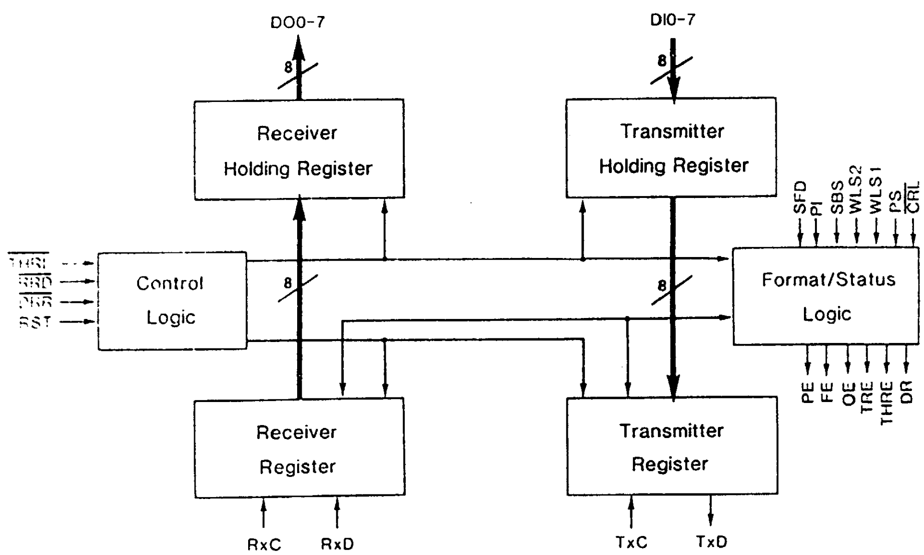


MODEL 2718
©CCS 1980
2 SERIAL + 2
PARALLEL I/O

APPENDIX B

UART/USART INTERNAL OPERATION

B.1 THE UART



UART BLOCK DIAGRAM

FIGURE B 1

B.1.1 UART Transmitter Cycle

A UART transmitter cycle begins when the processor pulls SAW* low. SAW*, through THRL*, shifts the character on the data bus into the Transmitter Holding Register (TxHR), and from there to the Transmitter Register (TxR) when transmission of the previous character has been completed. [For expansions of the signal mnemonics and descriptions of the signal functions, see Table B.1, pages

B-4 and B-5.] When THRL* goes high, THRE goes low. The transfer of data into the TxR is signaled by TRE going low and THRE going high again. TRE going low causes the generation of the start bit, the high-to-low transition of which signals the beginning of serial data transmission over TRO. TRE goes high again when the stop bit has been transmitted, enabling the transfer of the next character from the TxHR. The new character can be loaded into the TxHR anytime after THRE goes high, and so may be loaded before transmission of the previous character is completed.

UART TRANSMITTER TIMING

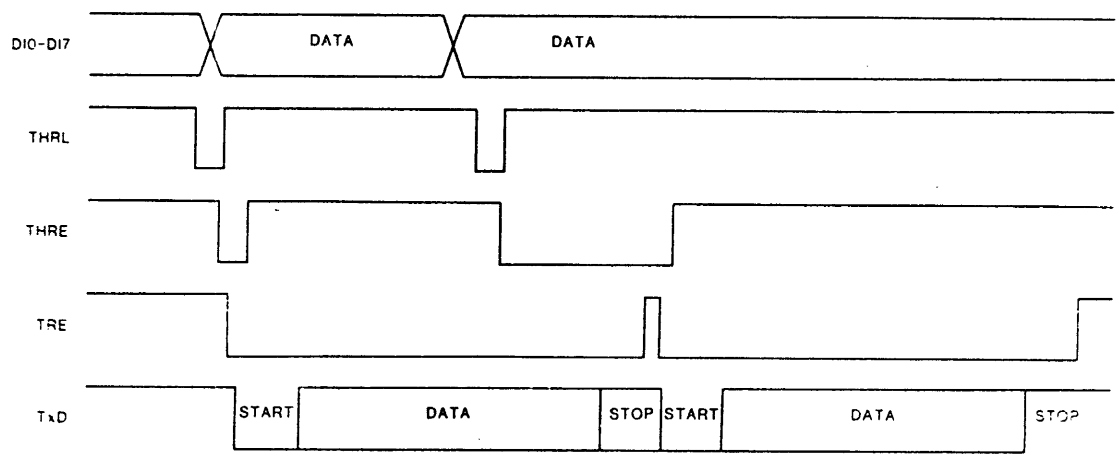


FIGURE B 2

B.1.2 UART Receiver Cycle

The processor begins a receiver cycle by pulling SAR* low. If the DR output is low, indicating that the RxHR is empty, RTS will be forced high, signaling to the peripheral

UART RECEIVER TIMING

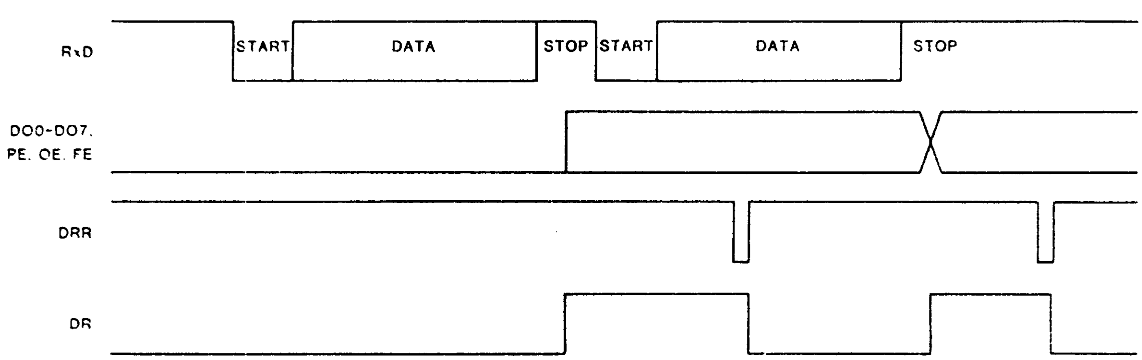
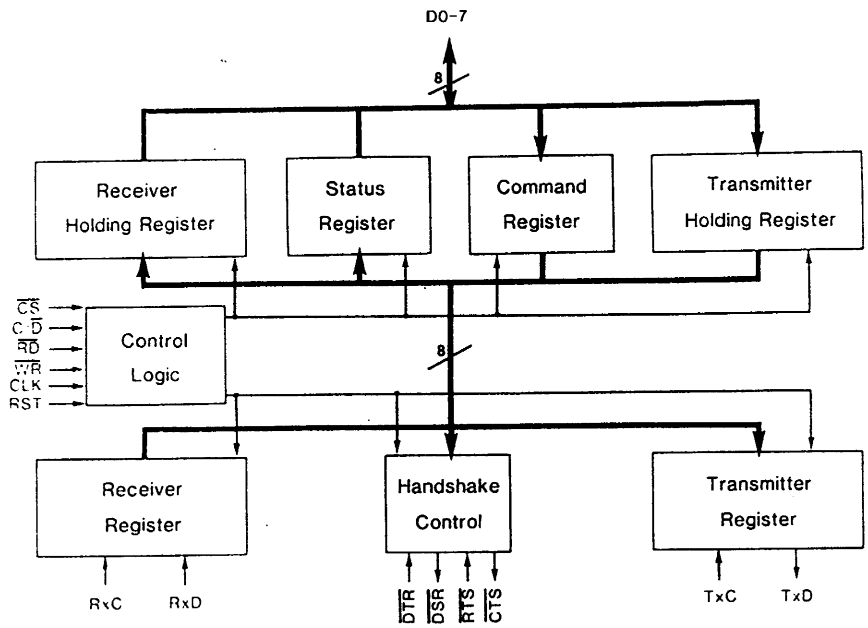


FIGURE B.3

that the UART is ready to receive. If DR is high, it is reset by the NANDing of DR high and SAR* low inverted high. SAR* low also enables, through RRD*, data transfer from the Receiver Holding Register (RxHR) onto the 2718 data bus. Thus RTS is forced high at the same time that a character is gated from the RxHR onto the 2718 data bus. Serial data is sent to the Receiver Register (RxR) least significant bit first, and is then transferred to the RxHR. The high-to-low transition of the start bit synchronizes the UART to the incoming data. Data in the RxHR is valid for one character time, after which it may be overwritten by the next character.

B.2 THE USART



USART BLOCK DIAGRAM

FIGURE B 4

B.2.1 USART Transmitter Cycle

The USART transmitter cycle is controlled by Bit 5 of the command word. A 1 in Bit 5 forces CTS* low. This signal, inverted, tells the peripheral to prepare to receive. The peripheral responds by forcing RTS high; inverted, this signal enables output from the USART through RTS*. Internal logic controls the transfer of data from the 2718 data bus through the TxHR and TxR onto TxD.

B.2.2 USART Receiver Cycle

Bit 1 of the command word controls the receiver cycle. A 1 in Bit 1 forces DSR* low. This signal, inverted, informs the peripheral that the USART is ready to receive. The peripheral responds by toggling DTR*; this signal controls no internal logic, however, acting only as a flag. Internal logic controls the transfer of the data through the registers onto the 2718 data bus.

TABLE B.1

UART PIN #	USART PIN #	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
-	1,2,27, 28,5-8	D0-7	DATA 0-7 connect the internal 8-bit bi-directional data bus of the USART with an external data bus.
5-12	-	DO0-7	DATA OUT 0-7 output receiver data in parallel to an external data bus.
26-33	-	DI0-7	DATA IN 0-7 input parallel transmitter data from an external data bus
20	3	RxD	RECEIVER DATA inputs serial data from a peripheral device to the Receiver Register.
25	19	TxD	TRANSMITTER DATA outputs serial data from the Transmitter Register to a peripheral device.
17	25	RxC	RECEIVER CLOCK clocks data into the Receiver Register through RxD at the selected baud rate.
40	9	TxC	TRANSMITTER CLOCK clocks data from the Transmitter Register onto TxD at the selected baud rate.
34	-	CRL	CONTROL REGISTER LOAD high enables loading of the control bits (Pins 35-39).
35	-	PI	PARITY INHIBIT disables parity generation and verification and holds PE low.
36	-	SBS	STOP BIT SELECT determines the number of stop bits used.
38,37	-	WLS1,2	WORD LENGTH SELECT 1 and 2 determine the number of bits per word.
39	-	PS	PARITY SELECT determines whether parity, if not inhibited, will be odd or even.
13	-	PE	PARITY ERROR high indicates that the character in the Receiver Holding Register does not exhibit the proper parity.
14	-	FE	FRAMING ERROR high indicates that the character in the Receiver Holding Register has no valid stop bit.
15	-	OE	OVERRUN ERROR high indicates that DR was not reset before a new character was transferred to the Receiver Holding Register.
16	-	SFD	STATUS FLAG DISCONNECT high forces PE, FE, OE, DR, and THRE into the high-impedance state.
23	-	THRL	TRANSMITTER HOLDING REGISTER LOAD low causes a character to be loaded from DI0-7 into the Transmitter Holding Register. Loading will be delayed until transmission of the previous character into the Transmitter Register is completed.
22	-	THRE	TRANSMITTER HOLDING REGISTER EMPTY indicates that the transfer of a character from the Transmitter Holding Register to the Transmitter Register has been completed, and that a new character may be loaded into the Transmitter Holding Register.

Note: The RS-232-C signals RxD and TxD are named from the point of view of the data terminal device; thus data transmitted from the processor through the 2718's serial ports will be presented on interface line BB, RxD, while data to be received by the processor will be presented on line BA, TxD. Clock signals will also be oppositely designated by the RS-232-C specifications and the 2718 serial ports.

TABLE B.1 (cont'd)

UART PIN #	USART PIN #	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
24	-	TRE	TRANSMITTER REGISTER EMPTY indicates when high that the transmission of a character is completed. TRE goes low at the beginning of transmission.
4	-	RRD	RECEIVER REGISTER DECREMENT low enables output of parallel data from the Receiver Holding Register.
19	-	DR	DATA RECEIVED indicates the presence of a complete character in the Receiver Holding Register.
18	-	DRR	DATA RECEIVED RESET low clears DATA RECEIVED.
-	12	C/D	CONTROL/DATA determines whether the USART will be in a data or status/command mode.
-	10	WR	WRITE, when low, determines that a data or command write to the USART will take place.
-	13	RD	READ, when low, determines that data or status will be read from the USART.
-	20	CLK	CLOCK provides the internal timing for the USART. It does not control data transfer baud rates.
-	23	CTS*	CLEAR TO SEND inversely reflects Bit 5 of the Command, a low indicating that the USART is ready to transmit data.
-	17	RTS*	REQUEST TO SEND is used by the peripheral device to indicate that it is ready to receive data. A low enables transmission by the USART if Bit 0 of the Command is a 1.
-	24	DSR*	DATA SET READY inversely reflects Bit 1 of the Command, a low indicating that the USART is ready.
-	22	DTR*	DATA TERMINAL READY, used as a response to DTR and inversely reflected in USART status bit 7, indicates when low that the peripheral is ready.
21	21	RST	RESET clears the internal logic. The USART will remain in an idle state until re-initialized.
-	11	CS	CHIP SELECT high forces the USART's data buffers into the high-impedance state and forces -RD and -WR high to disable reading and writing.
1	26	V_{CC}	+5v
3	4	V_{SS}	Ground
2	-	V_{GG}	-12v

*The names of these two pairs of signals, as given in the Am8251 data sheet, have been switched to conform to the names of the handshake signals. The data sheet is written for the 8251 used as a data terminal device; on the 2718 it functions as a data set device.

Note that because the 2718 inverts these low-active 8251 handshake signals, the corresponding command and status bits reflect the actual handshake signals rather than their inverses.